US 6,282,630 B1

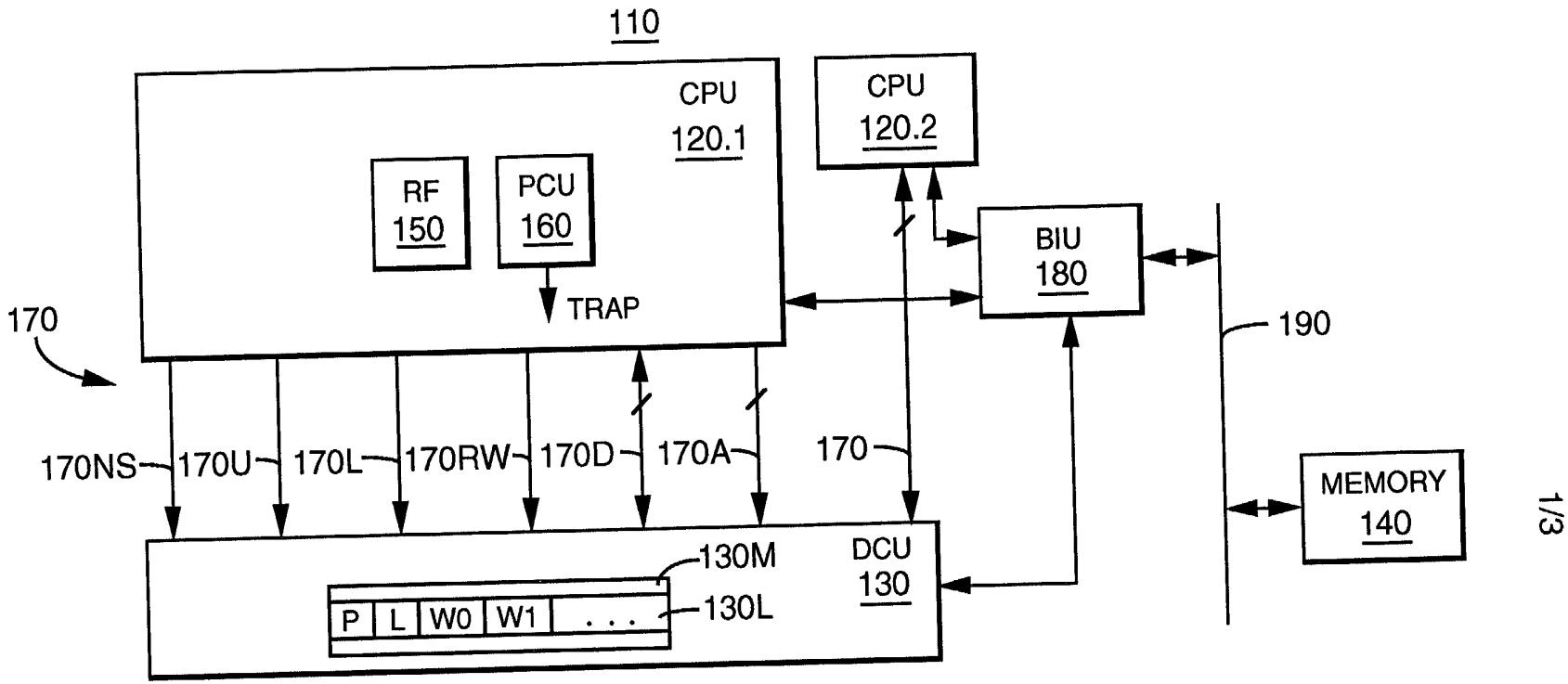

FIG. 1

F A D/R E C(A1) A2 A3 T WB
F A D/R E C(A1) A2 A3 T WB

FIG. 2

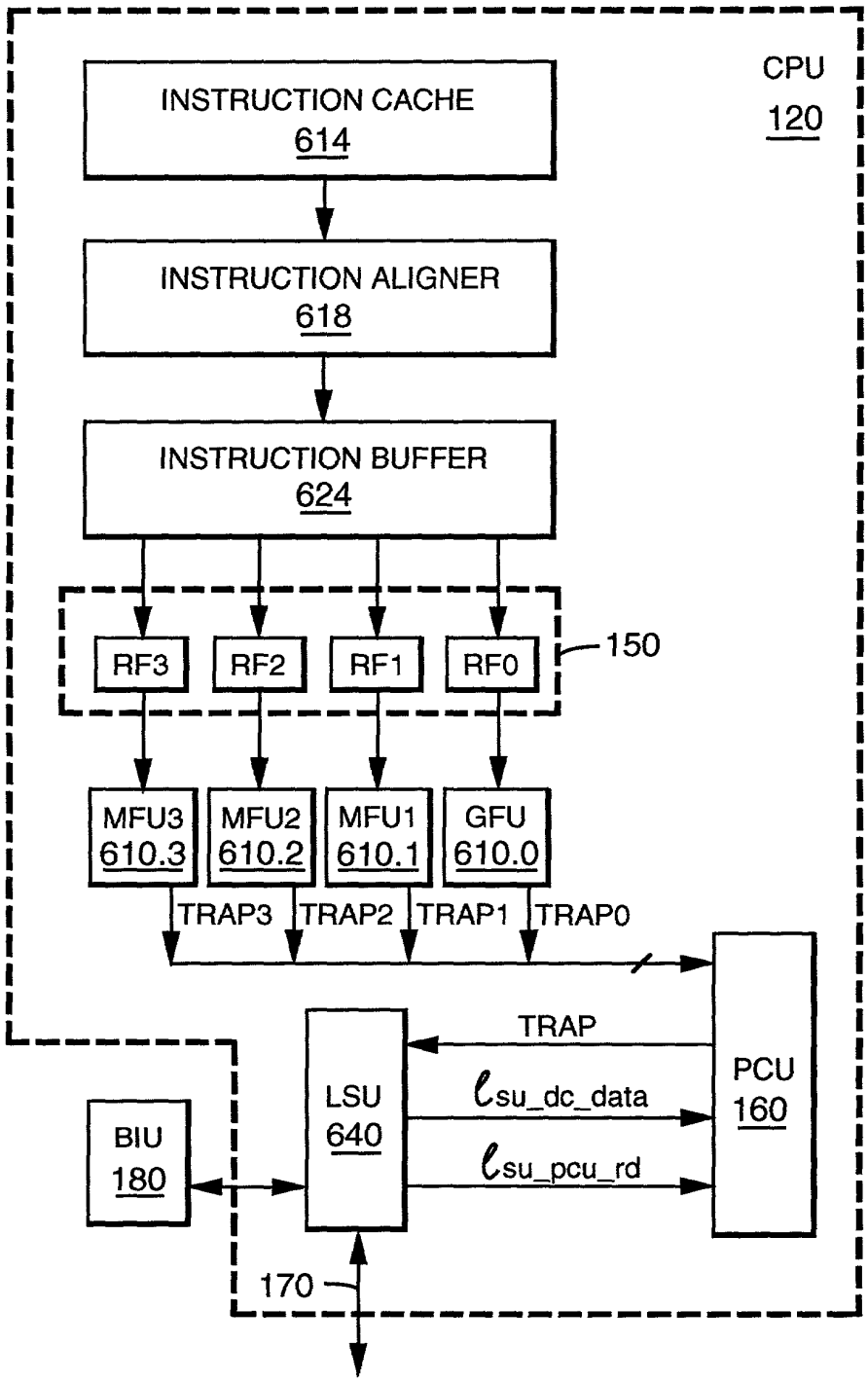
CPU
120
INSTRUCTION CACHE
614
INSTRUCTION ALIGNER
618
INSTRUCTION BUFFER
624
RF3
RF2
RF1
RF0
150
MFU3
610.3
MFU2
610.2
MFU1
610.1
GFU
610.0
TRAP3
TRAP2
TRAP1
TRAP0
TRAP
PCU
160
LSU
640
su_dc_data
su_pcu_rd
BIU
180
170

FIG. 3

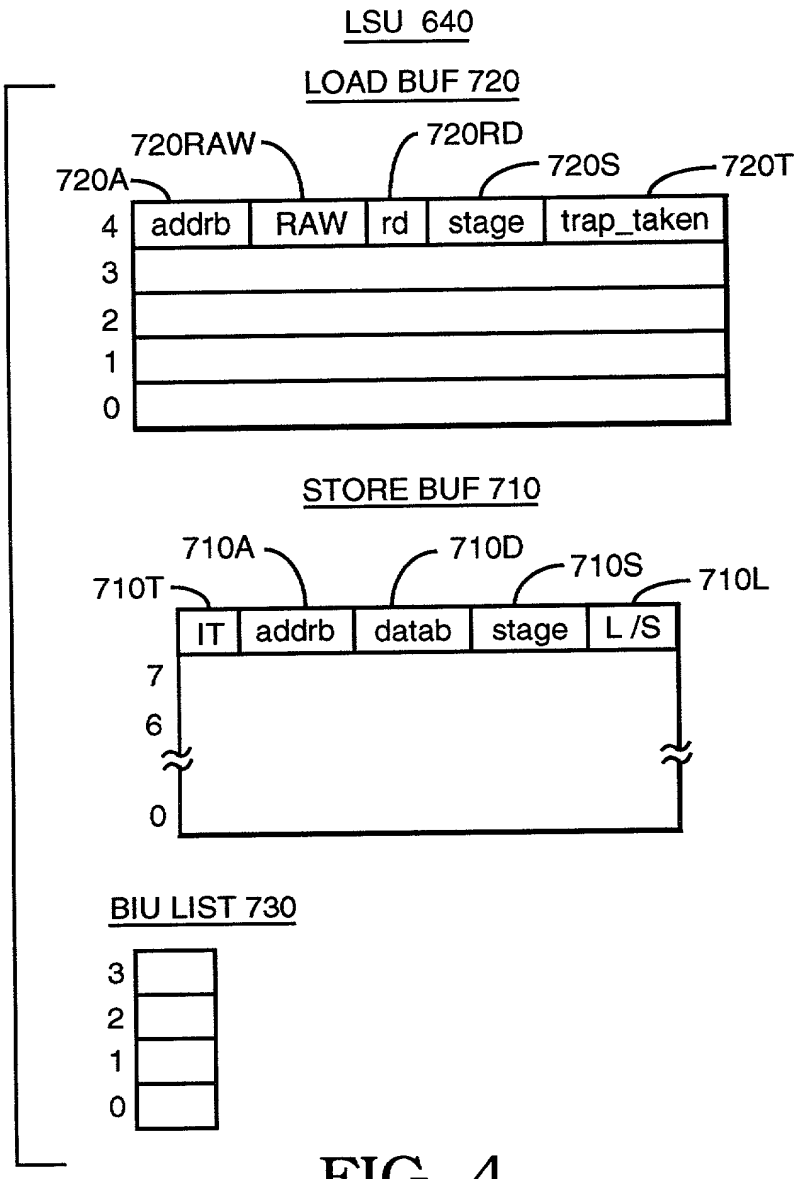
LSU 640
LOAD BUF 720
720RAW
720RD
720A
720S
720T
4
addrb
RAW
rd
stage
trap_taken
3
2
1
0
STORE BUF 710
710A
710D
710T
710S
710L
IT
addrb
datab
stage
L /S
7
6
0
BIU LIST 730
3
2
1
0

FIG. 4

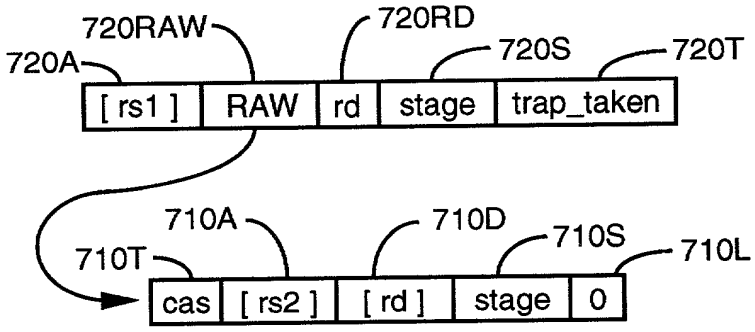
720RAW
720RD
720A
720S
720T
[rs1]
RAW
rd
stage
trap_taken
710A
710D
710T
710S
710L
cas
[rs2]
[rd]
stage
0

FIG. 5